REMARKS

This amendment is in response to the non-final Office Action mailed April 17, 2008. Claims 13, 16-18, and 24-31 are currently pending. Claims 1 and 3-23 stand rejected. Claims 13 and 16-18 have been changed, claims 1, 3-12, 14, 15, and 19-23 have been cancelled, and claims 24-31 have been added by this amendment. Reconsideration of the present application in view of the amendments and remarks that follow is respectfully submitted.

Applicant has amended claims 13, 16, and 17 and cancelled claims 1, 3-12, 14, 15, and 19-23 from further consideration in this application. Applicant is not conceding in this application that the original claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution. Applicant respectfully reserves the right to pursue the original and other claims in one or more continuations and/or divisional patent applications.

The amendments to the claims are fully supported by the specification. Claims 13, 24, and 29 recite that the first rotate up and rotate down signals and the second rotate up and rotate down signals are logically ORed to provide the phase adjusts, as described at page 5, lines 18-21 and Fig. 4. The other amendments include subject matter of previously existing claims. Therefore, no new matter has been added.

§112 Rejections

The Examiner rejected claims 12 and 18 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement, stating that the claims contain subject

matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention.

The Examiner stated that claims 12 and 18 recite that the "adder accumulates a chosen number of most significant bits of the rotate up and rotate down signals" while the specification shows Fig. 2's adder accumulating the chosen most significant bit of the up/down counter instead of the chosen most significant bits of the rotate up/down signals. Fig. 1 shows the adder 12 receiving the 11 most significant bits from the up/down counter. To clarify the claims and expedite prosecution, Applicant has amended claim 18 to recite that the chosen most significant bit of the up/down counter are accumulated, and respectfully requests that the rejection under 35 U.S.C. 112, first paragraph, be withdrawn.

§102 Rejections

The Examiner rejected claims 1, 3-11, 13-17, and 19-23 under 35 U.S.C. §102(b) as being anticipated by Fujii, U.S. Patent No. 5,349,309 ("Fujii"). Applicant respectfully traverses, and has amended the claims for clarification and to expedite prosecution.

Fujii discloses a phase locked loop including a random walk filter, a counter, a register, and an adder. An internal counter in the random walk filter provides an UP or DOWN signal to the counter when the internal count gets to –N or +N. The counter emits a count value to the adder which adds the count value and a value from the register, and emits the result to an oscillating circuit.

Fujii does not disclose or suggest the invention of claim 13. Claim 13 recites phase adjusts including first rotate up and down signals based on accumulated phase adjust data accumulated by an up-down counter and adder, and generates future adjusts

including second rotate up and rotate down signals improving a rate of compensation for the frequency offsets. The first rotate up and rotate down signals and the second rotate up and rotate down signals are logically ORed to provide the phase adjusts to the reference clock. Fujii does not disclose or suggest generating second rotate up and rotate down signals, where the first rotate up/rotate down and the second rotate up/rotate down signals are logically ORed to provide the phase adjusts of the clock signal. The Examiner stated that Fujii discloses second rotate up and rotate down signals as the output of the adder 6. But the output of adder 6 is provided directly to the oscillator 7 and is not ORed with first rotate up and rotate down signals to provide phase adjusts. Applicant therefore believes that claim 13 is patentable over Fujii.

Dependent claims 16-18 are dependent on claim 13 and are patentable over Fujii for at least the same reasons as claim 13, and for additional reasons. For example, claim 17 recites generating the second rotate down signal based on an underflow in the adder. Fujii does not disclose or suggest detection of underflow in the adder. The Examiner states that Fujii discloses logic generating a new rotate down signal based on an overflow and/or underflow in the adder, in the case when the counter 4 has a count value at +M or –M, the counter emits the count value to the adder as the n-bit signal. However, counter 4 does not only emit a count value only at –M or +M, but appears to emit every count value that it keeps (col. 4 lines 45-54; col. 4, lines 7-9; Fig. 5 shows no emitting at only –M and +M). This is not an overflow or underflow signal detected in the adder 6 or counter 4.

Applicant therefore believes that claims 13, 16, and 17 are patentable over Fujii. Accordingly, Applicant respectfully requests that the rejection under 35 U.S.C. 102(b) be withdrawn.

103 Rejections

The Examiner rejected claims 12 and 18 under 35 U.S.C. 103(a) as being unpatenable over Fujii. Applicant respectfully traverses. Claim 18 is dependent from claim 13, which is believed patentable over Fujii as explained above. Claim 18 is thus patentable over Fujii for at least the same reasons, and for additional reasons. Applicant therefore believes that claim 18 is patentable over Fujii, and respectfully requests that the rejection under 35 U.S.C. 103(a) be withdrawn.

New Claims

New claim 24 is a method claim including subject matter similar to that of former claim 1, and recites adapting the first rotate up and down signals for phase adjusts based on accumulated data accumulated by an adder, and generating second rotate up and rotate down signals improving a rate of compensation for the frequency offsets. The first rotate up and rotate down signals and the second rotate up and rotate down signals are logically ORed to provide the phase adjusts of the clock signal. Fujii does not disclose or suggest the logical ORing of two rotate signals as explained above with reference to claim 13. Thus claim 24 is believed patentable over Fujii for at least similar reasons to those explained above for claim 13. Dependent claims 25-28 recite subject matter similar to former claims 3-6 and are patentable over Fujii for at least the same reasons as claim 24 and for additional reasons. For example, claim 28 is patentable for reasons similar to those explained above for claim 17.

New claim 29 is a method claim including subject matter similar to that of former claims 7-11, and recites using an adder that outputs accumulated data indicative of a trend in the phase adjustments, and combinatorial logic to adapt the rotate up and rotate down signals based on the accumulated data. The combinatorial logic generates a new

rotate up signal based on an overflow in the adder and the combinatorial logic generates a new rotate down signal based on an underflow in the adder. As explained above with reference to claim 7, Fujii does not disclose or suggest overflow and underflow in the adder. Counter 4 does not only emit a count value only at –M or +M, but appears to emit every count value that it keeps (col. 4 lines 45-54; col. 4, lines 7-9; Fig. 5 shows no emitting at only –M and +M). This is not an overflow or underflow signal detected in the adder 6. Applicant therefore believes that claim 29 is patentable over Fujii.

Claims 30 and 31 are dependent from claim 29 and are patentable over Fujii for at least the same reasons as claim 29, and for additional reasons. For example, claim 31 recites that the rotate up and rotate down signals and the new rotate up and rotate down signals are logically ORed to provide the phase adjusts of the clock signal, which is patentable over Fujii as explained above with reference to claim 13.

For the reasons stated hereinabove, Applicants respectfully assert that all claims, as presented in the Amendment, stand ready for allowance and request a Notice of Allowance be timely provided.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, the Examiner is invited contact the undersigned at the telephone number indicated below.

Respectfully submitted,

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May 29, 2008
Date

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